THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

MCCORKLE, JOHN W., et al.

Application No.: 09/685199

Filed: 10-10-2000

Docket No.: XSI014

Patent No.: 6975665 B1

Issue Date: 12-13-2005

Examiner: Shuwang Liu

Group Art Unit: 2634

Title: LOW POWER, HIGH RESOLUTION TIMING GENERATOR FOR ULTRA-WIDE

9999999

BANDWIDTH COMMUNICATION SYSTEMS

Certificate of Submission

I hereby certify that this correspondence is being submitted to the USPTO, Alexandria, VA.

- Addressed per C.F.R. § 1.1(a) and deposited with the United States Postal Service with sufficient postage as first class mail.
- Facsimile transmitted in accordance with C.F.R. §1.6(d).
- Submitted electronically via EFS in accordance with "Legal Framework for EFS Web".

May 29, 2008
Date of Submission

-/44

Signature

Printed Name of Person Signing Certificate

Commissioner for Patents Alexandria, VA 22313

SUBMISSION OF CERTIFICATE OF CORRECTION

Dear Commissioner:

Enclosed is a Certificate of Correction listing error(s) in the subject patent.

Please enter these corrections. Since the errors appear to be on the part of the United States Patent Office, there should be no charge.

Respectfully submitted,

SINGH,/RANJEEY

Attorney for Applicant(s) Registration No. 47093

Telephone No. (512) 996-6839 Facsimile No. (512) 996-6854

PTO/SB/ 44 (04-05)
Approved for use through 04/30/2007 OMB 0651-0033
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

Page	1_	of _	4
------	----	------	---

PATENT NO .:

6975665 B1

APPLICATION NO:

09/685199

DATE:

10-10-2000

FIRST NAMED INVENTOR:

MCCORKLE, JOHN W.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In Column 24, Line 44, Claim No. 1:

Change "signal in frequency;" to--signal in frequency,--

In Column 24, Line 46, Claim No. 1:

Change "a plurality of high frequency clock signals;" to--a plurality of high frequency clock signals,--

In Column 24, Line 48, Claim No. 1:

Change "plurality of low frequency control signals;" to--plurality of low frequency control signals,--

In Column 25, Line 55, Claim No. 9:

Change "frequency clock signals;" to-- frequency clock signals,--

In Column 25, Line 59, Claim No. 9:

Change "the agile timing signal in frequency; and" to--the agile timing signal in frequency, and--

In Column 27, Line 16, Claim No. 20:

Change "modulating the agile timing signal in frequency base on a" to-modulating the agile timing signal in frequency based on a--

In Column 28, Line 12, Claim No. 25:

Change "high frequency clock signals;" to--high frequency clock signals,--

In Column 29, Line 30, Claim No. 33:

Change "generation circuit;" to--generation circuit,--

In Column 29, Line 32, Claim No. 33:

Change "high frequency clock signals;" to--high frequency clock signals,--

In Column 29, Line 34, Claim No. 33:

Change "low frequency clock signals;" to--low frequency clock signals,--

In Column 29, Line 43, Claim No. 33:

Change "signals via the controller; and" to--signals via the controller, and--

In Column 29, Line 60, Claim No. 34:

Change "generation circuit for the tuning" to--generation circuit for fine tuning--

In Column 30, Line 57, Claim No. 41:

Change "signals via the control means;" to--signals via the control means,--

In Column 30, Line(s) 62-63, Claim No. 41:

Change "phase relationships respectively such that the first" to--phase relationships, respectively, such that the first--

Page 3 of 4

In Column 32, Line 4, Claim No. 49:

Change "clock signals via the controller;" to--clock signals via the controller,--

In Column 33, Line 31, Claim No. 57:

Change "tuning of the agile signal in frequency" to--tuning of the agile timing signal in frequency--

In Column 34, Line 47, Claim No. 65:

Change "generation circuit;" to--generation circuit,--

In Column 34, Line 49, Claim No. 65:

Change "high frequency clock signals;" to--high frequency clock signals,--

In Column 34, Line 51, Claim No. 65:

Change "low frequency clock signals; and" to--low frequency clock signals, and--

In Column 34, Line 60, Claim No. 65:

Change "controller;" to--controller,--

In Column 34, Line 61, Claim No. 65:

Change "wherein the low frequency con generation" to--wherein the low frequency control generation--

In Column 35, Line 3, Claim No. 66:

Change "of the agile-timing signal in frequency." to—of the agile timing signal in frequency.--

In Column 36, Line 8, Claim No. 73:

Change "signals via the control means;" to-signals via the control means,--

Page <u>4</u> of <u>4</u>
In Column 37, Line 24, Claim No. 81:
Change "frequency clock signals via the controlled;" to—frequency clock signals
via the controller,
In Column 38, Line 48, Claim No. 89:
Change "via the controller; and" to—via the controller, and
Change via the controller, and to the way a via

MAILING ADDRESS OF SENDER (Please do not use customer number below)
Freescale Semiconductor, Inc.

Freescale Semiconductor, Inc. Law Department 7700 West Parmer Lane PL02 Austin, TX 78729